Electromagnetic wave sensors

Low-Power, High-Sensitivity Readout Integrated Circuit With Clock-Gating, Double-Edge-Triggered Flip-Flop for Mid-Wavelength Infrared Focal-Plane Arrays

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Abstract—To facilitate a high-dynamic-range operation of mid-wavelength infrared focal-plane arrays, a low-power, high-sensitivity readout integrated circuit (ROIC) is proposed. In this ROIC, the capacitor-reset block employing clock signals adopts a double-edge-triggered flip-flop instead of a single-edge-triggered one to reduce errors within the final output signals. In addition, an asynchronous clock-gating technique is employed to control clock-signal usage in accordance with the input signal, thereby reducing the power consumption within two-dimensional arrays. The proposed low-power, high-sensitivity ROIC has been realized with a 0.18-μm 1-poly 6-metal CMOS process. It has been confirmed that in cases involving low input-signal current, the power consumption of the proposed ROIC can be reduced to approximately 2% of that of conventional ROICs.

Index Terms—Electromagnetic wave sensors, sensor interface electronics, clock gating, double-edge-triggered flip-flop, mid-wavelength infrared (MWIR), readout integrated circuit (ROIC).

I. INTRODUCTION

Mid-wavelength infrared (MWIR) focal-plane arrays employed in defense applications, such as missile systems [missile seeker, IR search and track], must meet the requirements of high dynamic range, low power consumption, high sensitivity, and so on [1]–[4]. A high-dynamic-range readout integrated circuit (ROIC) characterized by an asynchronous self-controlled two-gain-mode operation and multiple reset control in accordance with the input signal for each pixel was recently proposed [5]. To facilitate high-dynamic-range operation in this ROIC, a 10-MHz clock signal was used to generate a 100-ns pulse signal that resets the integration capacitor. This pulse width, albeit small, may cause an error to exist within the final output signal. This implies that the occurrence of an integration time difference of 100 ns between similar input signals may cause differences to exist within the output signal. Meanwhile, in conventional high-dynamic-range ROICs, a clock signal is provided as input to all pixels regardless of the input signal. However, when the input-signal current is low, the use of the clock signal becomes redundant, thereby resulting in excessive, unwarranted power consumption of ROICs.

In this study, the use of a capacitor-reset block employing a double-edge-triggered (DET) flip-flop instead of a single-edge-triggered (SET) one is proposed to facilitate the reduction of errors within the final output signal. In addition, the use of an asynchronous clock-gating technique in combination with ROIC internal signals is proposed to reduce power consumption within 128 × 128 arrays. The utility of the proposed circuit was demonstrated through post-layout simulations.

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II. CIRCUIT IMPLEMENTATIONS AND ANALYSIS RESULTS

A. Capacitor-Reset Block With DET D Flip-Flop (DFF)

In the conventional high-dynamic-range ROIC, a capacitor-reset block [shown in Fig. 1(a)] comprising a one-bit latch, SET-DFF, and NAND gate was employed to reset the integration capacitor (C_{int}) as well as generate a single pulse, the width of which equals one clock cycle [5]. When the voltage ($V_{\text{cap\_out}}$) of the integration-capacitor output signal exceeds the reference voltage (V_{ref}) during the integration period, the output signal (V_{comp}) of the comparator becomes "1" and a capacitor-reset signal (V_{HDR}) is generated at the rising edge of the clock signal (10 MHz). However, the voltage (V_{HDR}) of the capacitor-reset output signal may possess a delay of up to 100 ns depending on the operating timing of the output signal ($V_{\text{cap\_out}}$) relative to the reference voltage (V_{ref}), as shown in Fig. 1(b). If the integration-capacitor output signal exceeds the reference voltage just before a rising edge of the clock signal, such as the case of $V_{\text{cap\_out1}}$, it is reset immediately. However, if the integration-capacitor output signal exceeds the reference voltage just after a rising edge of the clock signal, such as the case of $V_{\text{cap\_out2}}$, it is reset at the next rising edge of the clock signal. This implies that there may be an integration time difference up to 100 ns between similar input signals. Consequently, an integration time difference can lead to an output-signal difference. The larger the input-signal current is, the greater the difference in the output signal will be.

In general, a 20-MHz clock signal can be used to reduce errors within the final output signal. However, such high-frequency clock signals may cause problems, such as noise interference and excessive power consumption. To overcome these concerns, this study proposes the use of a capacitor-reset block employing a DET-DFF instead of SET-DFF. Several types of DET-DFFs exist [6]–[8]. Compared to other DET-DFFs, a single-phase-clocked DET-DFF in [7] was observed to

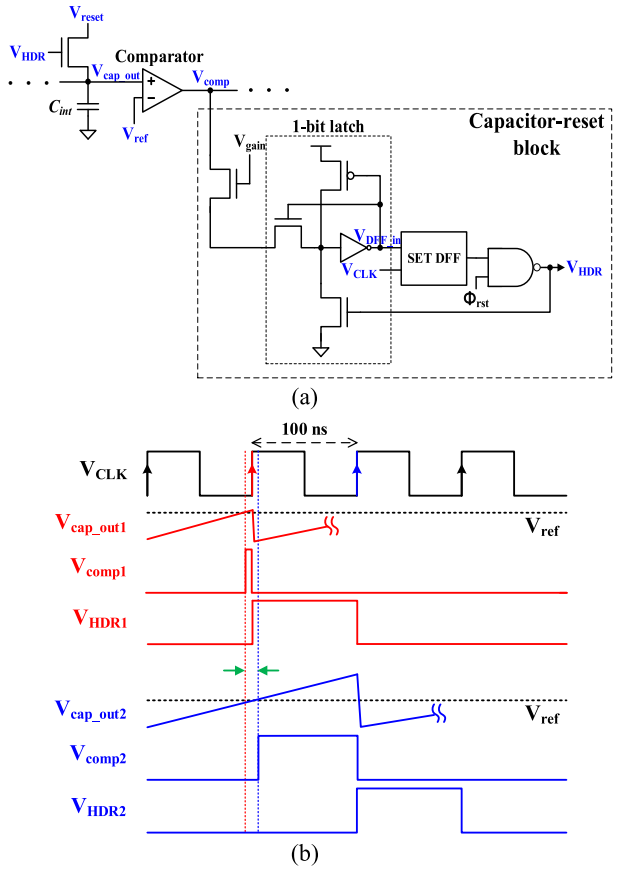

Fig. 1. Configuration of the conventional high-dynamic-range ROIC. (a) Schematic diagram of capacitor-reset block. (b) Operation timing diagram of the conventional ROIC.

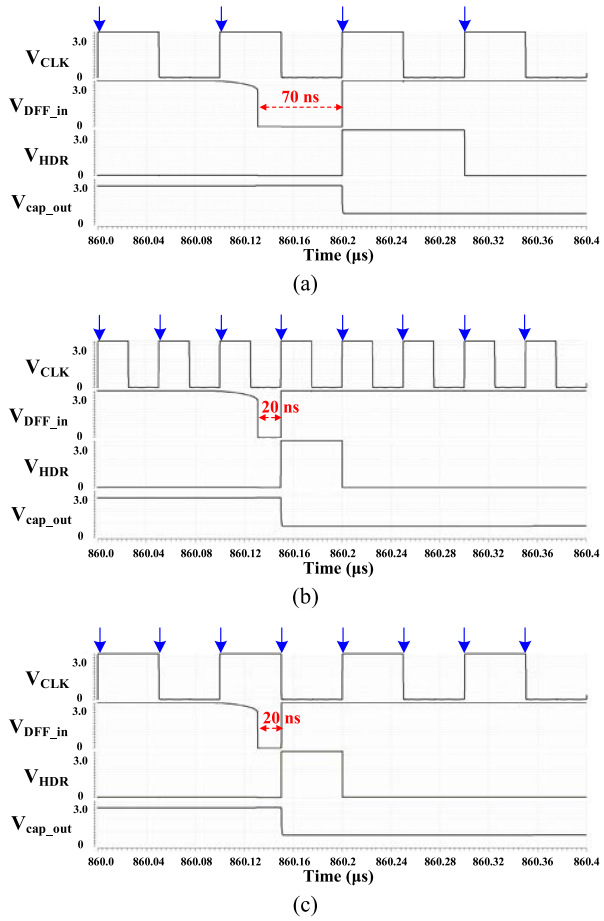

Fig. 2. Simulation results of the high-dynamic-range ROIC. (a) Capacitor-reset block with SET-DFF (10-MHz clock). (b) Capacitor-reset block with SET-DFF (20-MHz clock). (c) Capacitor-reset block with DET-DFF (10-MHz clock).

reduce both the total transistor count and number of clocked transistors per flip-flop. Therefore, this DET-DFF was employed in the proposed ROIC considering the stable operation of ROIC and pixel pitch of a small area. Fig. 2 shows the simulation results of high-dynamic-range ROICs with SET-DFF or DET-DFF-equipped capacitor-reset blocks. As can be observed in the figure, the SET-DFF-equipped capacitor-reset-block uses 10-MHz and 20-MHz clock signals, and the DET-DFF-equipped capacitor-reset block uses a 10-MHz clock signal. Under conditions of a high-input signal current, the signal V_{comp} is input to DFF when the output voltage of the integration capacitor exceeds the reference voltage. Since the SET-DFF-equipped capacitor-reset block (10-MHz clock) can be triggered on only one edge, the output signal is reset after 70 ns, regardless of the activation of $V_{\text{DFF\_IN}}$. However, because the DET-DFF-equipped capacitor-reset block (10-MHz clock) is triggered on both edges of the clock signal, the output signal is reset after 20 ns. The delay related to the capacitor-reset signal (V_{HDR}) results in the occurrence of errors within the final output signal. The DET DFF with a 10-MHz clock [see Fig. 2(c)] can have almost the same effect as the SET DFF with a 20-MHz clock [see Fig. 2(b)], so that two circuits have a delay of less than 50 ns. Thus, errors within the final output signal can be reduced via the use of a DET-DFF-equipped capacitor-reset-block.

In the case of an SET-DFF-equipped capacitor-reset block with a 10-MHz clock, the delay has a maximum value of 100 ns. A delay error of 100 ns, which is approximately 1/30 000 of the total integration time (3 ms), can induce a delay error noise of up to 66.7 μV (@ $V_{\text{out\_swing}} =$ 2.0 V). On the other hand, in the case of a DET-DFF-equipped capacitor-reset block with a 10-MHz clock, the delay has a maximum value of 50 ns. A delay error of 50 ns, which is approximately 1/60 000 of the total integration time (3 ms), can induce a delay error noise of up to 33.3 μV (@ $V_{\text{out\_swing}} = 2.0$ V). Consequently, the delay error noise ($V_{\text{error\_noise}}$) of the SET-DFF- and DET-DFF-equipped capacitor-reset blocks is estimated to be 66.7 and 33.3 μV, respectively.

B. Asynchronous Clock-Gating Technique

As already mentioned, capacitor-reset blocks equipped with a clock signal required for ROIC operation generate pulse signals for resetting the integration capacitor. In conventional high-dynamic-range ROICs, because multiple resets of the integration capacitor are performed asynchronously for each pixel during the integration period, clock signals are provided as input to all pixels regardless of the input signal. With regard to approaching missile targets, if the target is at a long distance, most pixels operate in the high-gain mode, because the input-signal level is low. In such cases, the use of the clock signal in capacitor-reset block becomes unnecessary and may even result in system malfunctioning and/or increased ROIC power consumption. To address these concerns, an asynchronous clock-gating technique is proposed in this letter. Clock gating is an efficient way of reducing the overall power consumption in digital systems and selectively deactivating the clock signal [9], [10].

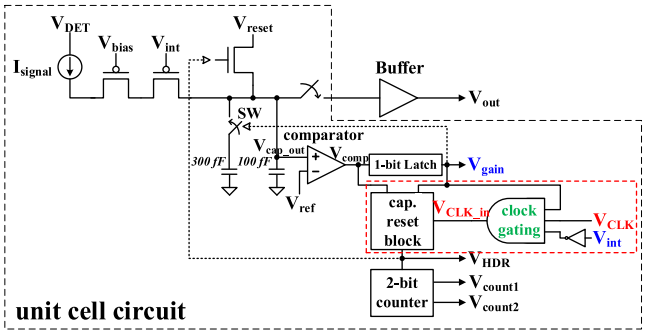

Fig. 3. Schematic of the proposed unit cell circuit.

Table 1. Operating Modes of the Proposed High-Dynamic-Range ROIC.

V_{gain}	V_{count2}	V_{count1}	Operating Mode	Input signal current
0	0	0	High-gain mode	~ 67 pA
1	0	0	Low-gain mode	67 pA ~ 270 pA
1	0	1	HDR mode (one reset)	270 pA ~ 1.1 nA
1	1	0	HDR mode (two resets)	
1	1	1	HDR mode (three resets)	

Fig. 3 shows the proposed unit cell circuit employing the asynchronous clock-gating technique. As previously mentioned, the capacitor-reset block was designed with the DET-DFF. The proposed clock-gating technique can be employed to control the use of clock signals asynchronously in accordance with the input-signal current. The two clock-gating control signals (V_{gain} and V_{int}) are generated internally within the ROIC. The switch-enable signal (V_{gain}) is used to distinguish the low-gain mode from the high-gain mode at the system level, as shown in Table 1. When the switch-enable signal is high (i.e., $V_{gain} = 1$), multiple reset control of the 400-fF integration capacitor is performed. The integration-control signal (V_{int}) is used to control the integration time for all pixels within ROIC identically. When the integration-control signal is low (i.e., $V_{int} = 0$), photocurrent integration is performed. Likewise, if the switch-enable signal is low (i.e., $V_{gain} = 0$) or the integration-control signal is high (i.e., $V_{int} = 1$), the use of the clock signal becomes unnecessary. In this way, the proposed clock-gating technique serves to reduce the ROIC power consumption.

The conceptual diagram of four neighboring pixels and the layout design of the proposed unit cell circuit are shown in Fig. 4. In the layout design, the proposed circuit containing multiple functions cannot be easily integrated into one pixel with a pixel size of 15 μm × 15 μm. This pixel size is the most commonly used size in commercial MWIR detectors. As a result, four neighboring pixels (2 × 2 pixels) share the proposed unit cell circuit and the size of the unit cell circuit will subsequently be 30 μm × 30 μm. In addition, the four neighboring pixels and the proposed unit cell circuit are connected via the indium bump.

The post-layout simulation results of the proposed ROIC are shown in Fig. 5. As can be observed, one frame can be divided into the integration and read periods. During the integration period, the photocurrent from the detector is integrated on the integration capacitor.

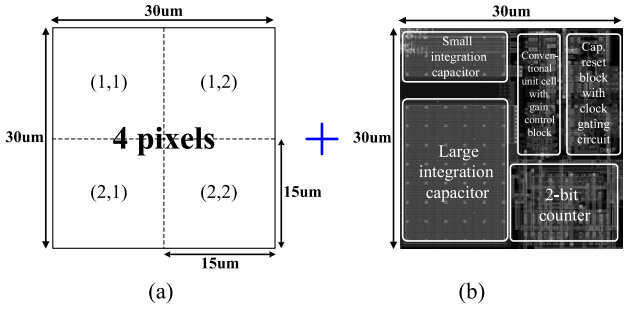

Fig. 4. (a) Conceptual diagram of four neighboring pixels (2 × 2 pixels). (b) Layout of the proposed unit cell circuit.

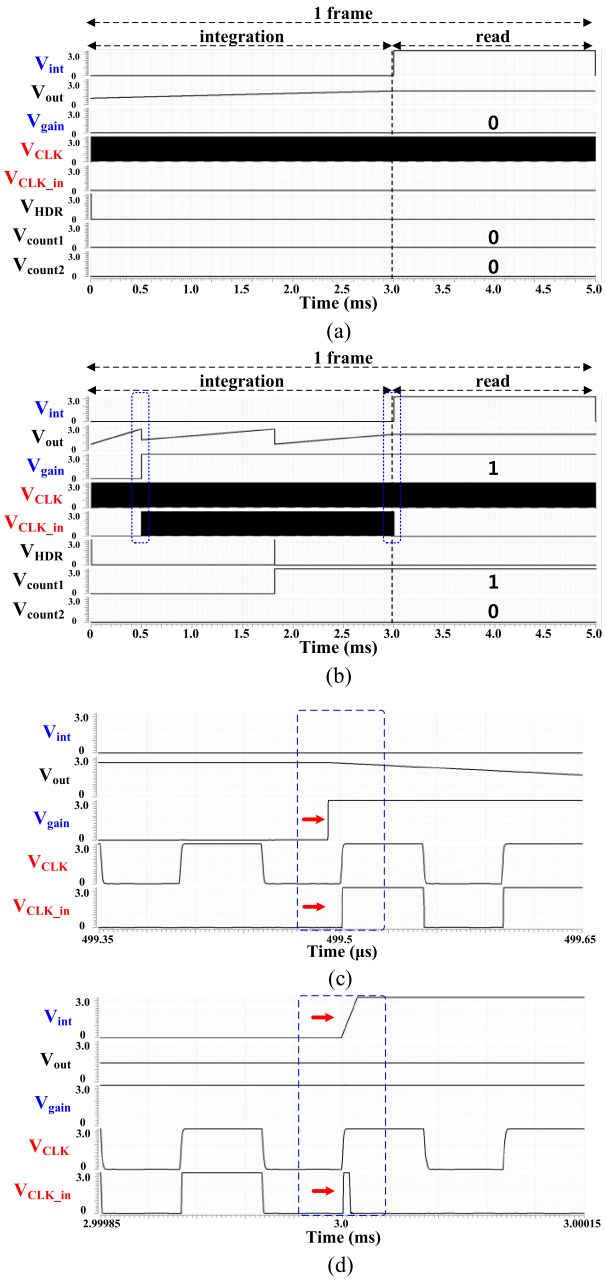

Fig. 5. Post-layout simulation results for the proposed high-dynamic-range ROIC. (a) High-gain mode. (b) HDR mode (one reset). (c) Clock signal activated in the HDR mode (one reset). (d) Clock signal deactivated in the HDR mode (one reset).

Table 2. Power-Consumption Comparison Results.

Operation Mode	[5] (10 MHz)①	[5] (20 MHz)②	Proposed ROIC (10 MHz)③		
	Power (mW)	Power (mW)	Power (mW)	Ratio (③/①)	Ratio (③/②)
High-gain mode	13.88	23.52	0.32	2.3%	1.4%
Low-gain mode	13.79	23.44	6.15	44.6%	26.2%
HDR mode (1 reset)	13.95	23.61	9.55	68.5%	40.4%
HDR mode (2 resets)	14.02	24.78	10.33	73.7%	41.7%
HDR mode (3 resets)	14.08	24.75	10.61	75.4%	42.9%

Table 3. Performance Comparison Results.

	[5] (10 MHz)	[5] (20 MHz)	Proposed ROIC (10 MHz)
Array size	128×128	128×128	128×128
Pixel pitch	15 μm	15 μm	15 μm
Full well capacity	20×10^6 e-	20×10^6 e-	20×10^6 e-
Dynamic range	99.2 dB	99.2 dB	99.2 dB
Delay error noise	66.7 μV	33.3 μV	33.3 μV
Power consumption (High-gain mode)	13.88 mW	23.52 mW	0.32 mW

The signal level at the end of the integration period is maintained, and the same is sent to the system during the read period. In the case of the high-gain mode [see Fig. 5(a)], the clock-signal input ($V_{\text{clk\_in}}$) is deactivated during one frame. In the case of the high-dynamic-range (HDR) mode with one reset [see Fig. 5(b)], when the switch-enable signal is high (i.e., $V_{\text{gain}} = 1$), the clock-signal input ($V_{\text{clk\_in}}$) to the capacitor-reset block is activated [see Fig. 5(c)], and a multiple-reset control of the 400-fF integration capacitor is performed. Additionally, when the integration-control signal is high (i.e., $V_{\text{int}} = 1$), the clock-signal input ($V_{\text{clk\_in}}$) to the capacitor-reset block is deactivated [see Fig. 5(d)].

C. Power-Consumption Comparisons

To verify the efficiency of the clock-gating technique, the power consumption by the proposed ROIC, which employs the asynchronous clock-gating technique, was compared to those by the conventional high-dynamic-range ROICs with 10-MHz and 20-MHz clocks.

Table 2 lists the results obtained upon comparison of the power consumed by the proposed 128 × 128 array ROIC with that consumed by conventional 128 × 128 array ROICs. In this study, the effect of only the capacitor-reset blocks equipped with the clock-gating circuit was considered for power consumption comparison. In the case of a very high input-signal current (HDR mode with three resets), the power consumed by the proposed ROIC can be reduced to 75.4% and 42.9% of that consumed by conventional ROICs equipped with 10-MHz and 20-MHz clocks, respectively. Further, in the case of a low input-signal current (high-gain mode), the power consumed by the proposed ROIC can be reduced to 2.3% and 1.4% of that consumed by the same conventional ROICs. Table 3 shows the performance comparison results of the conventional and proposed ROICs. The proposed ROIC has low-noise and low-power characteristics with high dynamic range.

III. CONCLUSION

This letter demonstrated the utility of a DET-DFF-equipped high-dynamic-range ROIC employing the asynchronous clock-gating technique. The DET-DFF-equipped capacitor-reset block serves to reduce errors within the final output signal, whereas the asynchronous clock-gating technique can reduce the power consumed by the proposed ROIC to roughly 2% of that consumed by conventional 128 × 128 array ROICs. In view of these findings, the proposed ROIC can be considered useful in missile-application systems requiring a high dynamic range of operation, low power consumption, and high sensitivity.

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